

WHAT IS CLAIMED IS:

1. A clock divider for a DLL (Delay Lock Loop) circuit of a synchronous memory device for synchronization of an external input clock with an internal input clock, the clock divider comprising:

M (where M is an integer that is larger than 2) dividers connected in series; and

a power-down controller for receiving an output signal of the (M-1)-th divider and an output signal of the M-th divider, and selectively outputting the output signals;

wherein the respective dividers divide a frequency of a clock signal inputted to the respective dividers into $1/2$.

2. The clock divider as claimed in claim 1, wherein the output signal of the power-down controller has a frequency obtained by dividing the frequency of the clock signal inputted to the first divider into $1/2^M$ or $1/2^{(M-1)}$ in accordance with a logic level of a control signal.

3. The clock divider as claimed in claim 2, wherein if the logic level of the control signal is a first state (high level), the output signal of the power-down controller becomes the output of the (M-1)-th divider, and if the logic

level of the control signal is a second state (low level), the output signal of the power-down controller becomes the output of the M-th divider.

5 4. The clock divider as claimed in claim 3, wherein the control signal is a clock enable signal used in the synchronous memory device.

10 5. The clock divider as claimed in any one of claims 1 to 4, wherein a pulse width of a high-level state of the output signal of the first divider is the same as a period of the input signal of the first divider, and a pulse width of a low-level state of output signals of the second to M-th dividers is the same as the period of the input signal of the
15 first divider.

20 6. The clock divider as claimed in claim 6, wherein the power-down controller comprises two transmission gates, and the two transmission gates are selectively turned on/off according to the control signal.

7. A clock dividing method for a DLL (Delay Lock Loop) circuit of a synchronous memory device for synchronization of an external input clock with an internal input clock, the

method comprising the steps of:

selectively outputting an output signal of a (M-1)-th divider and an output signal of an M-th divider among M dividers, connected in series, for respectively dividing a
5 frequency of the input clock signal into $1/2$.